IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Michael Trinh	
Serial No.:	09/256,643	Group Art Unit: 2822	
Filed:	February 23, 1999	Docket: 303.324US2	
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE		

#22/Response 1/12/02 MVarnell

RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

This response is accompanied by a Petition, as well as the appropriate fee, to obtain a one-month extension of the period for responding to the Office action, thereby moving the deadline for response from 23 October 2001 to 23 November 2001.

In response to the Office Action dated 23 July 2001, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 21, 23, 24, 26, 29-33 and 36-75 are pending in the application. Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are rejected, and claims 33, 47, 62, 67, 70, and 75 are objected to. None of the claims have been amended.

Allowable Subject Matter

The Examiner indicated that claims 33, 47, 62, 67, 70, and 75 would be allowable if rewritten in independent form. The applicant reserves the right to rewrite claims 33, 47, 62, 67, 70, and 75 in independent form, but believes that the base claims from which they depend are allowable in view of the remarks made herein.

Rejections Under 35 USC § 103

Claims 21, 23-26, 29-32, 36-46, and 48-59 were rejected under 35 USC § 103(a) as being unpatentable over Chamberlain (U.S. Patent No. 4,473,836) taken with Halvis et al. (U.S. Patent No. 5,369,040, Halvis). The applicant respectfully traverses.

Claim 43 recites a method of fabricating a transistor comprising, among other elements, forming a source region and a drain region in a substrate, forming an insulating layer on the

substrate, forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0, and removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

Chamberlain discloses a photodetector structure shown in Figure 2 including a silicon substrate 11 having a diffused photosensitive region D1 that functions as a source and a diffused region D2 that functions as a drain. Chamberlain, column 3, lines 10-15. When photosensing region D1 is illuminated, its voltage VD1 is a natural logarithmic function of the incident light. Chamberlain, text bridging columns 6 and 7. Chamberlain is deficient as a reference in that, as the Office Action stated, Chamberlain does not disclose forming a gate from a silicon carbide compound $Si_{1-x}C_x$ as recited in claim 43.

Halvis discloses a MOS photodetector with closely-spaced gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon. However, Halvis does not disclose forming a source region and a drain region in a substrate and forming an insulating layer on the substrate as recited in claim 43.

The Office Action stated that it would have been obvious to one of ordinary skill in the art to replace the gate of Chamberlain with the gate disclosed by Halvis. The applicant respectfully traverses.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143.

The Office Action stated on page 2 that it would have been obvious "to replace the polysilicon gate of Chamberlain with the gate of silicon carbide .... taught by Halvis .... because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity." These reasons are from the Office Action, not from either Chamberlain or Halvis as is required to establish a *prima facie* case of obviousness. Furthermore, there is no motivation for combining the teachings of Chamberlain and Halvis.

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." MPEP 2143.01. "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP 2143.01.

The modification of Chamberlain proposed in the Office Action would change the principle of operation of Chamberlain, and would render Chamberlain unsatisfactory for its intended purpose. Chamberlain states the following:

> "It is important to note that all parts of the photodetector structure are shielded from light except for region D1, the upper surface of which receives and is exposed to light." Chamberlain, column 3, lines 39-44.

However, the polysilicon and carbon gate of Halvis with which the Office Action proposes to replace the gate G1 of Chamberlain is transparent to visible light:

> "this invention describes a MOS photodetector which has gates fabricated from polysilicon with the addition of carbon .... which makes the gate material more transparent to the visible portion of the energy spectrum..." Halvis, column 2, lines 18-24.

If the gate G1 of Chamberlain were replaced by the transparent gate of Halvis as suggested in the Office Action, the principle of operation of the device of Chamberlain would be changed, and it would be unsatisfactory for its intended purpose of detecting incident light.

"To establish a *prima facie* case of obviousness ... there must be a reasonable expectation of success." MPEP 2143. The Office Action has **not** demonstrated that a device resulting from the combination of Chamberlain and Halvis would be successful, especially in view of the above-mentioned result of changing the gate of Chamberlain to be transparent to light, and therefore a *prima facie* case of obviousness has **not** been established.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 43 has **not** been established in the Office Action, and that claim 43 is in condition for allowance. Claims

44-46, 48, and 49 are dependent on claim 43, and recite further limitations with respect to claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 44-46, 48, and 49 has **not** been established in the Office Action, and that claims 44-46, 48, and 49 are in condition for allowance.

Claims 21, 23-26, 29-32, 36-42, and 50-59 recite limitations similar to those recited in claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 21, 23-26, 29-32, 36-42, and 50-59 are not disclosed or suggested by the combination of Chamberlain and Halvis, and that claims 21, 23-26, 29-32, 36-42, and 50-59 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,449,941, Yamazaki) in view of Halvis. The applicant respectfully traverses.

Claim 43 recites a method of fabricating a transistor comprising, among other elements, forming a source region and a drain region in a substrate, forming an insulating layer on the substrate, forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0, and removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

Yamazaki discloses in Figures 1A-1D and 2A-2D steps for forming memory cells with a source region in a substrate, a drain region in the substrate, an oxide film, a floating gate, and a control gate. Yamazaki is deficient as a reference in that, as the Office Action stated, Yamazaki does not disclose forming a gate from a silicon carbide compound $Si_{1-x}C_x$ as recited in claim 43.

Halvis discloses a MOS photodetector with closely-spaced gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon. However, Halvis does not disclose forming a source region and a drain region in a substrate and forming an insulating layer on the substrate as recited in claim 43.

The Office Action stated that it would have been obvious to replace the gate of Yamazaki with the gate taught by Halvis. The applicant respectfully traverses.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP 2143.01.

The Office Action stated on page 3 that it would have been obvious "to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide .... taught by Halvis .... because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity." These reasons are from the Office Action, and are not from either Yamazaki or Halvis as is required to establish a *prima facie* case of obviousness. There is no indication in Yamazaki that there are deficiencies that would be remedied by an addition from Halvis.

There are many reasons why one skilled in the art would not be motivated to combine Yamazaki and Halvis. The structures Yamazaki and Halvis are very different and operate in a different manner. Yamazaki discloses a memory device with a single floating gate. Halvis discloses a photodetector with multiple gates. There is no teaching that only one of the many Halvis gates comprising polysilicon and carbon would be advantageous in the structure of Yamazaki. Yamazaki does not have a gate of silicon carbide while Halvis does not have a source region or a drain region in a substrate. Yamazaki uses silicon carbide as an insulator between a drain and a floating gate, while Halvis uses polysilicon and carbon in a gate.

Furthermore, Yamazaki teaches away from the combination. Yamazaki includes a thin insulator 105 of silicon carbide formed selectively on a part of the drain 104 shown in Figures 1B to 1D. Column 4, lines 7-14 and 27-29 and column 6, lines 1-9. The silicon carbide insulator 105 is directly between the drain 104 and the floating gate 107. Yamazaki would not teach one skilled in the art to form either the floating gate 107 or the control gate 109 shown in Figure 1D from the same material as the insulator 105.

"To establish a *prima facie* case of obviousness ... there must be a reasonable expectation of success." MPEP 2143. The Office Action has not demonstrated that a device resulting from the combination of Yamazaki and Halvis would be successful, and therefore a *prima facie* case of obviousness has **not** been established.

The Office Action states on page 6 that Yamazaki discloses an EPROM cell that must be exposed to strong ultraviolet light to be erased, and this statement was made to establish a motivation to combine Yamazaki and Halvis. First, there are electrical methods of erasing an EPROM cell that do not require ultraviolet light, and the Office Action did not point to language in Yamazaki indicating that its cell is erased with ultraviolet light. Furthermore, the gate of Halvis is fabricated from polysilicon with the addition of carbon to make the gate material more transparent to the visible portion of the energy spectrum, not the ultraviolet portion of the spectrum. There is no indication that the gate of Halvis would help in the erasing of the EPROM cell of Yamazaki.

The applicant respectfully submits that a *prima facie* case of obviousness of claim 43 has **not** been established in the Office Action, and that claim 43 is in condition for allowance. Claims 44-46, 48, and 49 are dependent on claim 43, and recite further limitations with respect to claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that a *prima facie* case of obviousness of claims 44-46, 48, and 49 has **not** been established in the Office Action, and that claims 44-46, 48, and 49 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-42, 50-59, 60-61, 63-66, 68-69, and 71-74 recite limitations similar to those recited in claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 21, 23-24, 26, 29-32, 36-42, 50-59, 60-61, 63-66, 68-69, and 71-74 are not disclosed or suggested by the combination of Yamazaki and Halvis, and that claims 21, 23-24, 26, 29-32, 36-42, 50-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

Claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Halvis taken with Tohyama (U.S. Patent No. 5,858,811) and Chamberlain. The applicant respectfully traverses.

The applicant demonstrated above with respect to the rejection of claim 43 that there is no motivation to combine Halvis and Chamberlain. The Office Action has also not identified a sufficient motivation in the prior art to combine Tohyama with Halvis and Chamberlain. In view of the remarks listed above, the applicant respectfully submits that a *prima facie* case of obviousness of claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 has **not** been established in the Office Action, and that claims 21, 23-24, 26, 29-32, 36-46, 48-59, 60-61, 63-66, 68-69, and 71-74 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 21st day of November, 2001.

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